REMARKS

Claims 1-20 are all the claims pending in the application. Upon entry of this Amendment, claims 1, 4, 5, 17 and 19 are amended. No new matter is presented.

To summarize the Office Action, claims 1, 2, 4-14, 17 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Selwan et al. (U.S. Patent No. 5,526,025, hereinafter "Selwan") in view of Nakano et al. (U.S. Patent No. 6,043,818, hereinafter "Nakano") and Yamashita (U.S. Patent No. 6,313,844). Further, claims 19 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Okuda (U.S. Patent No. 6,380,689) in view of Nakano and Yamashita, and claims 15 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Selwan in view of Nakano and Yamashita, further in view of Ge et al. (U.S. Patent No. 5,347,292, hereinafter "Ge"). Claim 3 is objected to for depending from a rejected base claim, but would be allowable if rewritten in independent form to include all the limitations of the rejected base claim. The outstanding rejections are addressed as follows.

Claims 1, 2, 4-14, 17 and 18

Claims 1, 2, 4-14, 17 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Selwan in view of Nakano and Yamashita. This ground of rejection is traversed.

Initially, Applicant notes that the Examiner apparently refers to claim language in the alleged teachings Nakano and Yamashita which is not recited in the claims. Therefore,

Applicant respectfully requests that the Examiner refer to the claim limitations in their current form.

The Examiner's rejection notwithstanding, independent claims 1, 5 and 17 define a novel picture displaying apparatus and method of driving a picture displaying apparatus in which a plurality of memory cells store a unit display data of a part of a single display data, and a plurality of the unit display data stored in the plurality of memory cells are read from a memory unit in a first order and the plurality of the unit display data are read from the memory unit in at least one second order. Further, the plurality of unit display data read in said first order are written to the picture displaying unit as a first predetermined frame and the plurality of unit display data read in said at least one second order are written to said picture displaying unit as at least one second predetermined frame. The first predetermined frame and at least one second predetermined frame are displayed as different images by writing said plurality of unit display data to the picture displaying unit in said first order and said at least one second order.

Applicant submits that Selwan, Nakano and Yamashita, whether taken alone or in combination, fail to teach the features of these claims.

Selwan teaches a display controller which provides a reduction in bandwidth consumed by the display refresh process when static data is displayed on a computer screen. As taught by Selwan, all the display memory is read in a first pass and sent to the display, wherein the display data is analyzed to determine repetitions of the display data in sequentially consecutive memory locations and the repeat patterns are flagged and stored in a "tag memory". (Selwan at col. 3,

lines 43-62). In subsequent passes when the display is refreshed and the content of the display memory does not change (i.e., the same image is displayed over consecutive refresh cycles), the memory locations which contain repeating values are not accessed and the controller jumps to the next memory location which does not contain a repeating value, thereby reducing the memory bandwidth required for the display refresh process. (Selwan at col. 3, lines 62-65).

However, Selwan teaches that the tag memory must be updated each time the contents of the display memory change. (Selwan at col. 3, line 66 – col. 4, line 9). Thus, every time the image being displayed changes, the entire contents of the display memory must again be read to determine if repeating patterns in the new display image. Therefore, even assuming that the "first pass" and the subsequent retrieval of memory display items with the tag information indicating memory locations that can be skipped is a "first order" and "at least one second order" as alleged by the Examiner, the display data of Selwan is only read in a "second order" when the content of the display does not change (i.e., the same image is being displayed during refresh cycles).

Accordingly, Selwan clearly fails to teach a first predetermined frame and at least one second predetermined frame are displayed as different images by writing the unit display data to the picture displaying unit in said first order and said at least one second order because Selwan teaches that the unit display data is only read in the second order when the same image is displayed.

Nakano fails to compensate for the deficient teaching of Selwan. As noted in the previous Amendment, Nakano teaches a graphical user interface in which a rotating image is displayed by sequentially displaying a series of eighteen different bitmap images. (see Nakano at col. 13, line 52 – col. 14, line 20). According to Nakano, different display data (i.e., each of the different bitmap images) are read in sequence to provide the effect of a rotating icon. (see Nakano at col. 14, lines 8-10, "The bit-map data are read and displayed on display memory 76 ***in the order from No. 1 to No. 18***, so that icon 125 is easily displayed as if it is rotating clockwise.") (emphasis added). Thus, different display data (i.e., the different bitmap images) are read in the same sequence. In contrast, claims 1, 5 and 17 require that a plurality of unit display data is read in a first order and the plurality of unit display data is read in at least one second order. Therefore, even assuming that the eighteen different bitmap images are analogous to the claimed plurality of unit display data, Nakano clearly fails to teach reading display data in "at least one second order" because the bitmap images of Nakano are continuously read in the same sequence.

Nor does Yamashita compensate for the deficiencies of Selwan and Nakano. The Examiner contends that Yamashita teaches "memory read from the memory unit with memory cells in different order for each single frame or each plural predetermined frames." (Office Action at page 4). Applicant disagrees with the Examiner's interpretation of Yamashita.

Yamashita merely teaches a refresh controller for a storage device with a dynamic random access memory which requires a refresh for memory retention due to charge dissipation

in the memory cells. (Yamashita at col. 1, lines 38-43). According to Yamashita, an image signal is written to a first memory in a first blanking interval and an image signal is written to a second memory in a second blanking interval. (Yamashita at col. 2, line 61 – col. 3, line 13). Thus, the image signal may be read from the first memory while the image signal is being written to the second memory. (Yamashita at col. 12, lines 3-20). However, there is no suggestion that the order of reading the first memory is in any way different from the order in which the second memory is read, nor does Yamashita suggest that the order is different for each frame.

Thus, even assuming *arguendo* that motivation to combine the teachings of Selwan, Nakano and Yamashita is proper, the combination fails to teach all the limitations of independent claims 1, 5 and 17, at least for the reasons discussed above. Accordingly, reconsideration and withdrawal of the rejection of claims 1, 5 and 17 is requested. Further, Applicant submits that claims 2, 4, 6-14 and 18 are allowable at least by virtue of depending from claims 1, 5 and 17, respectively, and allowance of claims 2, 4, 6-14 and 18 is therefore requested.

Further, with respect to claim 4, Applicant disagrees with the Examiner's contention that Nakano teaches "part of the plurality of unit display data is changed" as claimed. As noted above, Nakano merely teaches that a series of bitmap images are simply displayed in a single sequence. Also, for the reasons discussed above, Yamashita fails to teach the features of claim 4 which are deficient in Nakano, as Yamashita fails to suggest a first order and at least one second order for reading the memory cells. Moreover, Applicant notes that claim 4 recites the subject

matter of claim 3, which the Examiner indicated as containing allowable subject matter. Claim 4 is presently amended only to correct for a grammatical error, which is not believed to change the scope of the claim. Thus, claim 4 should be allowable for similar reasons.

Claims 19 and 20

Claims 19 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Okuda in view of Nakano and Yamashita. This ground of rejection is traversed.

Claim 19 defines a method of driving a display apparatus in which a plurality of read unit display data are written to a picture displaying unit in said first order as a first predetermined frame and said plurality of read unit display data are written to said picture displaying unit in said at least one second order as at least one second predetermined frame. Claim 19 further requires that the first predetermined frame and the at least one second predetermined frame are displayed as different images by writing the unit display data to the picture displaying unit in said first order and said at least one second order.

Okuda merely teaches an active matrix luminescent type display panel including an analog to digital converter which samples an analog input signal and stores the analog signal as digital pixel data. The digital pixel data are read from a memory and written to the display. (Okuda at col. 3, lines 31-58 and col. 6, lines 44-58).

Further, as discussed above, Nakano teaches that different display data (i.e., the different bitmap images) are read in the same sequence. In contrast, claim 19 requires that a plurality of unit display data is read in a first order and the plurality of unit display data is read in at least one

second order. Applicant's previous arguments with respect to the deficient teaching of Nakano are equally applicable to the instant grounds of rejection.

As discussed previously Yamashita teaches that an image signal is written to a first memory in a first blanking interval and an image signal is written to a second memory in a second blanking interval. (Yamashita at col. 2, line 61 – col. 3, line 13). Thus, the image signal may be read from the first memory while the image signal is being written to the second memory. (Yamashita at col. 12, lines 3-20). However, there is no suggestion that the order of reading the first memory is in any way different from the order in which the second memory is read, nor does Yamashita suggest that the order is different for each frame, as discussed above with respect to the rejection of independent claims 1, 5 and 17.

Thus Okuda, Nakano and Yamashita, whether taken alone or in combination, fail to teach or suggest all the limitations of claim 19. Accordingly, reconsideration and withdrawal of the rejection of claim 19 is requested. Further, claim 20 is allowable at least by virtue of depending from claim 20, and allowance of claim 20 is therefore requested.

Claims 15 and 16

Claims 15 and 16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Selwan in view of Nakano and Yamashita further in view of Ge. Applicant submits that claims 15 and 16 are allowable at least by virtue of depending from claims 1 and 5, respectively. Accordingly, allowance of claims 15 and 16 is requested.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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